ABSTRACT OF THE DISCLOSURE

An inverted-phase detector is implemented in a system including a first clock circuit that provides a first clock signal and a delayed clock circuit that outputs an delayed clock signal. A reference circuit outputs a reference signal. A feedback circuit generates a feedback signal that is one of greater than and less than the reference signal when the first clock signal changes state before the second clock signal, and that is the other of greater than and less than the reference signal when the first clock signal changes state after the second clock signal.